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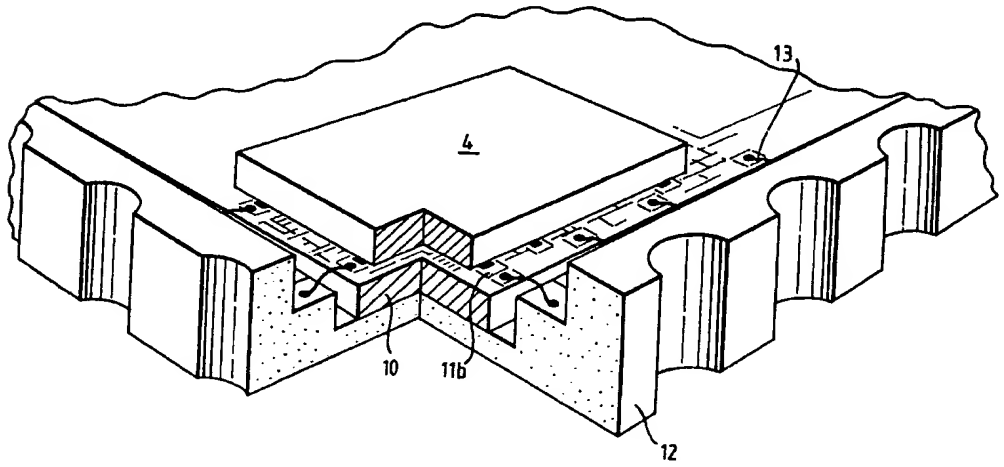
(54) Mounting integrated circuit devices

(57) A method of mounting and interconnecting electronic integrated circuits 4 comprises the steps of preparing a substrate 10 of substantially insulating semiconductor material eg Si, forming metallised interconnection conductor patterns 11 on said substrate, said patterns having surface connection areas 11b, attaching one or more electronic integrated circuits 4 to the substrate whereby the circuits make electrical contacts with certain of said connection areas, mounting the semiconductor substrate on a printed circuit structure or carrier 12 and forming electrical connections between other surface connection areas 11b and the printed circuit or carrier.

Fig.2.



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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

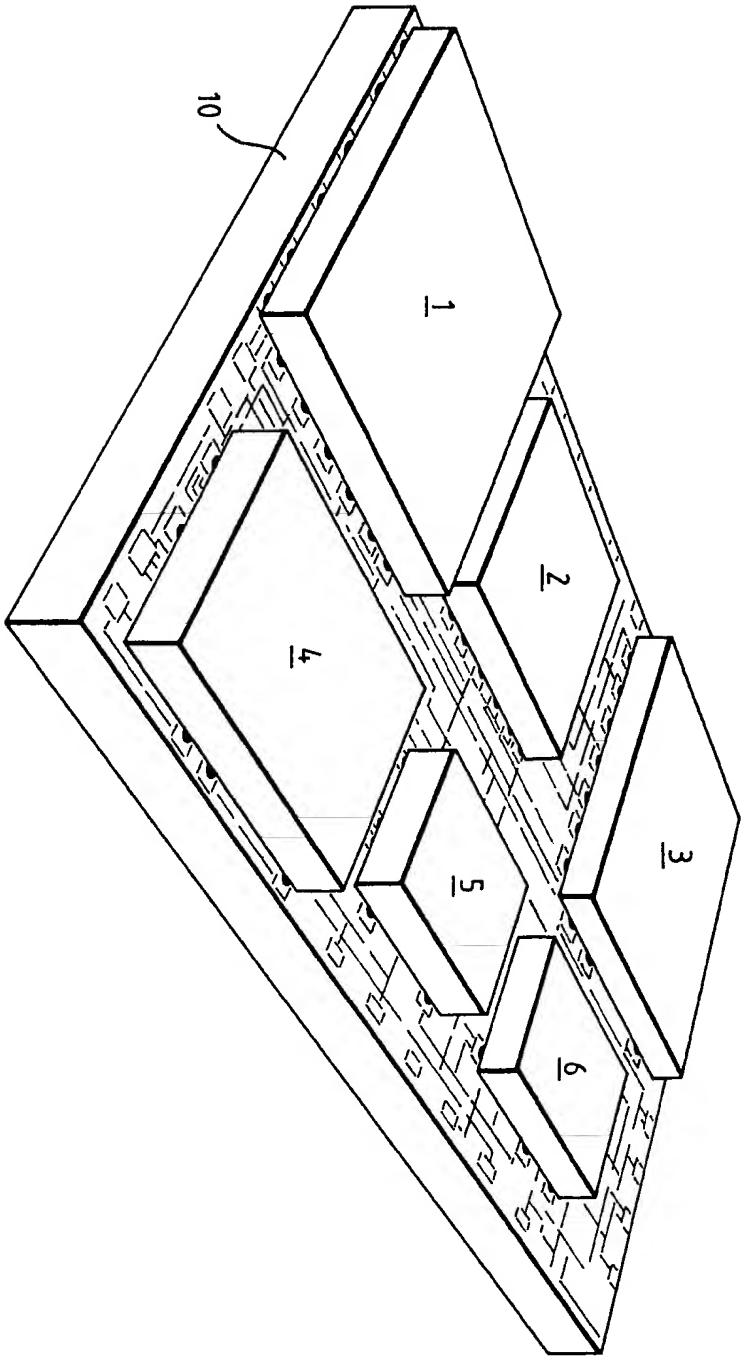

Fig.1.

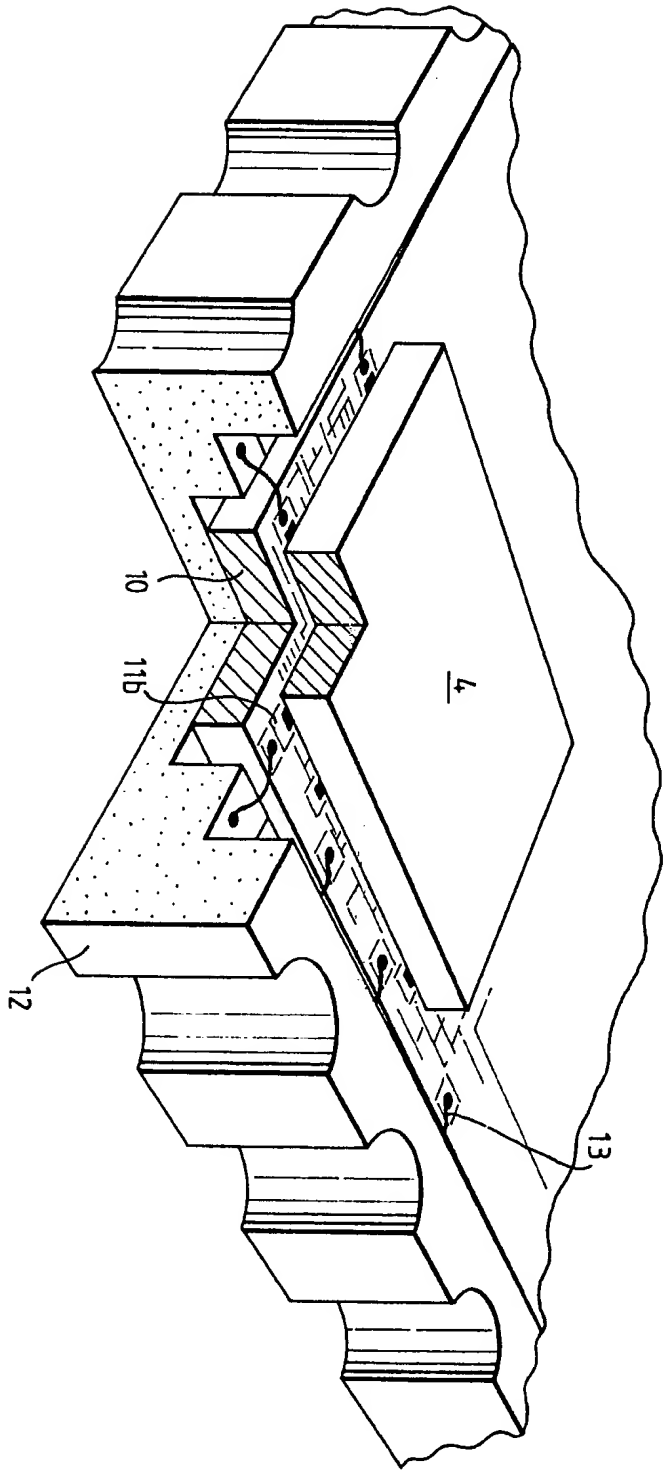

Fig.2.

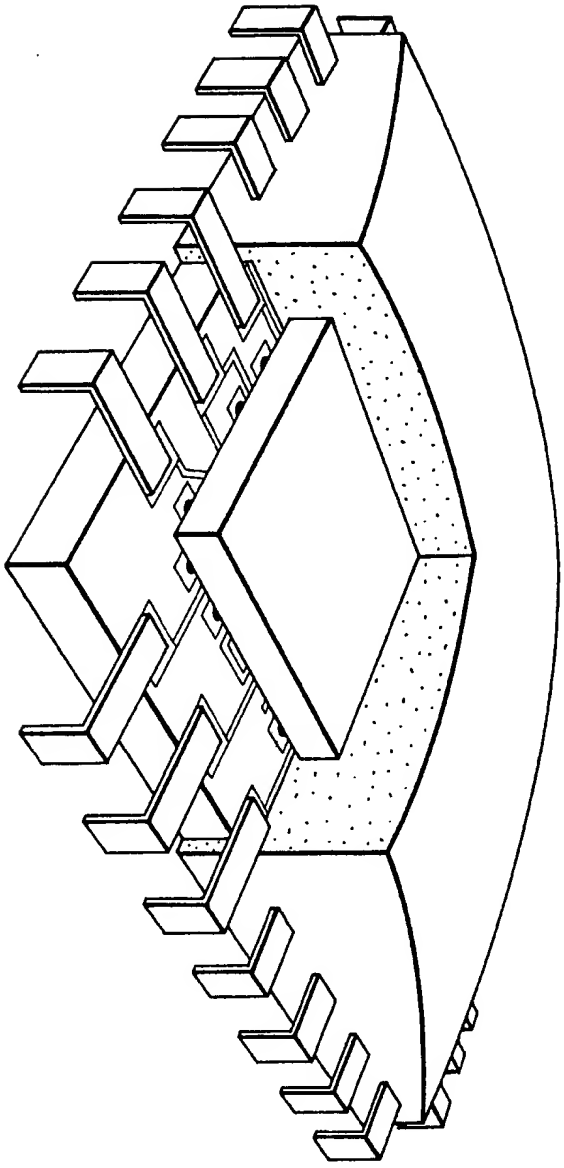

Fig.3.

SPECIFICATION

Mounting integrated ircuit devic s

This invention relates to the mounting and interconnection of integrated circuits.

Integrated circuits, either packaged or unpackaged (bare) "chips" are usually mounted on and interconncted by a printed circuit, e.g. a metallised conductor pattern formed on an insulating substrate, a ceramic or porcelain coated metal. However, it is clear that the printed circuit and the integrated circuit are, in the electronics field at least, at almost opposite ends of the interconnection spectrum.

The chip on the one hand is an extremely advanced and well developed piece of technology which has evolved rapidly both with respect to its electrical capabilities and its physical state, i.e. reliability, cost etc. On the other hand the printed circuit, although recently of substantially higher quality and improved technology generally, remains only a moderately advanced extension of its former self. Certainly the materials available have improved and a wider range of board materials and track characteristics are now available.

Conceptually, however, the technology is the same. Efforts to bring the chip into a working relationship with the printed board (PCB) have resulted in a variety of holding, packaging and clamping devices among which are the dual in-line package, the flat pack, the quad in-line package, the automatically bonded tape and the ceramic and plastic carriers, to name a few.

A common feature of most of the known devices of this type lies in the fact that they serve primarily as a "size" interface between the chips and the PCB. In other words, the carrier, packaged chip, etc. all effectively increase the size of the chip to a level compatible with current PCB handling and production technology.

This approach is very convenient for established production facilities. It does not, however, advance the technology of integrated circuit handling and interconnection nor does it allow for a solution which might have an even greater reliability and cost advantage.

According to the present invention there is provided a method of mounting and interconnecting electronic integrated circuits comprising the steps of preparing a substrate of substantially insulating semiconductor material, forming metallised interconnection conductor patterns on said substrate, said patterns having surface connection areas and attaching electronic integrated circuits to the substrate, whereby the circuits make electrical contacts with certain of said connection areas and other connection areas are available for electrical connections to external circuitry.

According to one aspect of the invention there is provided an interconnection substrate for electronic circuits comprising a body of substantially insulating semiconductor material on which are formed metallised interconnection conductor patterns having connection areas whereby electronic circuits can be attached to the substrate with electrical connections to certain of the connection areas whilst others of the connection areas are available for electrical connections to external circuitry.

Embodiments of the invention will now be described with reference to the accompanying drawings, in which:—

Figure 1 illustrates a number of electronic integrated circuits mounted on and interconnected by a semiconductor substrate,

Figure 2 illustrates an assembly of integrated circuits on a semiconductor substrate packaged in a carrier frame, and

Figure 3 illustrates packaging of an assembly of electronic circuits on a substrate within a conformal coating of an embedding compound.

In the arrangement shown in Fig. 1 a number of integrated electronic circuit 'chips' 1–6 are shown soldered to an interconnecting substrate of semiconductor material 10. The term 'chip' is used to denote a single body of semiconductor material, e.g. silicon, in which there are formed so-called 'integrated' circuits. Such circuits are formed by various well-known techniques, such as diffusion, expitaxial growth, ion implantation etc. The chip usually has metallised conductor patterns on the surface by means of which various interconnections between circuits in the chip are made and to which connections with external circuitry can be made. Hitherto, as explained above, chips are commonly mounted on and connected to printed circuits.

To promote higher packaging densities and reduce stress, the chips in Fig. 1 are mounted on and interconnected by the substrate 10 which is made of a semiconductor material, e.g. silicon, having the same or similar physical characteristics as the semiconductor material of the chips. The substrate semiconductor material may be either high-resisitivity p-type or n-type material, or may even be intrinsically insulating pure material. Interconnecting conductor patterns 11 are formed on the surface of the substrate 10 using conventional integrared circuit technology, e.g. the deposition of aluminium conductive tracks. The pattern 11 includes pad areas 11a which are aligned to allow connection with corresponding connection pad areas on the chips. Further connection pad areas 11b are provided to allow interconnection between the substrate 10 and a printed circuit board (not shown). The absence of electronic circuit elements formed in the substrate provides extra possibilities for improved deposition criteria and/or thicker connection pad areas. Such a

structure also allows the integrated circuit designer to place input/output connection pad areas to suit more important criteria than those required by conventional wire bonding techniques.

Fig. 2 illustrates an assembly of chips 4, 5 etc on a silicon substrate 10 packaged into a carrier 12, which may itself be leaded or leadless. Connections between the substrate pad areas 11b and the carrier are illustrated as wire bonds 13 but could equally well be by other conventional methods, such as lead frame. Additional pad areas can be incorporated to permit probe testing of the circuits once mounted.

Attachment of the integrated circuit chips is possible, using known technology. Solder 'bumps' may be provided on both the chips and the substrate so that when the solder is melted by the application of reflow heat surface tension in the molten solder accurately aligns the chips on the substrate. The use of either a tin/lead solder or an aluminium solder can be considered, the latter having the advantage of a lower melting point due to the small amount of silver included. Such an arrangement also improves the heat flow from the chips into the substrate to facilitate heat dissipation. Due to the fact that the integrated circuit chips and the substrate are of the same or similar materials the problems of differential expansion and contraction, as experienced in other chip mounting systems, are substantially eliminated.

The module thus formed is a fairly rugged entity and can be sealed into a package with a conformal coating of a suitable potting compound, as shown in Fig. 3. In this example the substrate 10 with its chips 4 etc is provided with leads 14 for subsequent attachment to a printed circuit board. The whole is then potted in a resin compound 15. The invention has the advantage that it uses proven technology and can be implemented using existing plant. Using the same materials and techniques as those used in chip production the substrates can be manufactured in sizes compatible with chip dimensions, thus achieving increases in circuit densities with a corresponding reduction in track density and/or layer count.

CLAIMS

1. A method of mounting and interconnecting electronic integrated circuits comprising the steps of preparing a substrate of substantially insulating semiconductor material, forming metallised interconnection conductor patterns on said substrate, said patterns having surface connection areas and attaching electronic integrated circuits to the substrate, whereby the circuits mak electrical contacts with certain of said connection areas and other connection areas are available for electrical connections to ext rnal circuitry.

2. A method according to claim 1 wherein the integrated circuits ar attached to the substrate by soldering.

3. A method according to claim 2 wherein the integrated circuits or the substrate are provided with solder bumps so that when the solder is melted by the application of reflow heat surface tension in the molten solder automatically aligns the circuits on the substrate.

4. A method according to claim 1, 2 or 3 wherein the substrate is a silicon slice with aluminium conductive tracks.

5. A method according to claim 4 wherein the conductor patterns on the substrate include additional contact areas to permit probe testing of the circuits once mounted.

6. A method according to any preceding claim wherein the substrate is packaged into a carrier with interconnection between the substrate and the carrier being effected by wire bonds.

7. A method according to any one of claim 1–5 wherein the substrate is packaged into a lead frame carrier.

8. A method according to any one of claim 1–5 wherein the substrate is mounted on and electrically connected to a printed circuit structure.

9. A method according to any preceding claims wherein the substrate carrying the integrated circuits is sealed in a potting compound.

10. A method of mounting and interconnecting electronic integrated circuits substantially as described with reference to the accompanying drawings.

11. An interconnection substrate for electronic circuits comprising a body of substantially insulating semiconductor material on which are formed metallised interconnection conductor patterns having connection areas whereby electronic circuits can be attached to the substrate with electrical connections to certain of the connection areas whilst others of the connection areas are available for electrical connections to external circuitry.

12. A substrate for electronic circuits substantially as described with reference to the accompanying drawings.

13. An assembly of electronic integrated circuits mounted on a substrate of substantially insulating semiconductor material, the substrate having formed thereon metallised conductor patterns, whereby the integrated circuits are interconnected, and connection areas whereby it can be electrically connected to a printed circuit or other structure carrying the substrate.

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